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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,345	02/09/2004	Hiroki Kanai	500.43504X00	9927

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EXAMINER	
CHERY, MARDOCHEE	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 04/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/773,345	HIROKI KANAI, SHOFI KATO, YUUSUKE YAUCHI	
	Examiner	Art Unit	
	Mardochee Chery	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/09/04,09/14/04,*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to Application No. 10/773345 filed on February 9, 2004.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-6, 9-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiozaki et al. (4,683,533) in view of Yamagami et al. (2002/0194435).

As per claims 1 and 9, Schiozaki et al. discloses a storage control apparatus in a storage system comprising receiving information processing apparatus and performing a data first storage control apparatus for data input/output request from an input/output process relative to a first storage volume storing data and a second storage control apparatus connected to a first storage control apparatus communication enable state for performing a data a second storage a input/output process relative volume for storing data, a first storage control apparatus comprises first memory for storing data transferred between a first storage control apparatus and a second storage control apparatus; [*a storage control system*; col.1, lines 6-8; *a transfer request received is compared with an MS request from another processor (including input/output units)*; col.4, lines 9-12; *a first control storage (address array) and second control storage (address array)*; col.2, lines 1-3; *for a write (store) operation by another processor to the main storage, a request is issued to the second address array (control*

storage) and thereafter the first address array (control storage) is updated; col.2, lines 12-16; *a first processor executes a store request on a main storage conducting communications with another system and a second processor fetches data stored*; col.2, lines 24-28]; a second memory [*a second address array for storing data*; col.1, lines 51-52]; an input/output control unit for writing data transfer information a second memory, a data transfer information containing a storage location data in a first memory and a storage location data a second storage control apparatus [*a block transfer request received via the line 13a is compared with an MS request from another processor (including input/output units) for accessing the MS 3 in the SCU 2*; col.4, lines 9-13; *the SCU 2 has a line 16a connected to the first address array controller 4awhich is used to indicate a transfer from the MS 3 to the BS 6a; the SCU is connected to a second address array controller 7a associated with the processor 1a and to a second address array controller 7b*; col.4, lines 19-26]; and a data transfer control unit having a data buffer for storing data, a data transfer control unit controlling data transfer between a first memory and a second storage control apparatus via a data buffer in accordance with a data transfer information read from a second memory and written in a data transfer register, wherein, when a second data transfer based on second data transfer information controlled while a first data transfer based on first data transfer information controlled, a data transfer control unit writes a first data transfer information stored in a data transfer register and data stored in a data buffer into a second memory, reads a second data transfer information from a second memory, writes a second data transfer information in a data transfer register, and in accordance with a second data transfer information, controls a second data transfer [*controllers 7a and 7b being provided with buffer address arrays*; col.4, lines 27-29; *a storage control system comprising a first buffer address array as a buffer storage directory for registering thereto an address of data copied from a shared storage into a buffer storage of each processor and a second buffer address array provided for a store address check requested from another processor;* col.1, lines 8-15; *access request in*

the second processor is accepted when a transfer from the shared storage to the buffer storage of the second processor is completed and the first buffer address array is updated in association with the transfer; col.3, lines 31-36; *the processor accesses the buffer storage onto which data stored in the main storage*; col.1, lines 25-27; *data is read from the buffer memory; a transfer is executed from the main storage to the buffer storage*; col.2, lines 39-42].

However Schiozaki et al. does not specifically teach a data transfer register for storing data transfer information as recited in the claim.

Yamagami et al. discloses and a data transfer register for storing data transfer information [*registers 340a and 340b are provided in correspondence to the respective SM access paths 125 and communication with the SM unit 160 can be ensured by reading/writing the registers 340a and 340b*; Fig.3, REG#0-REG#7; par.105, lines 1-6] to temporally store data of the storage units (par.3, lines 5-6).

Since the technology for implementing a storage control apparatus with a data transfer register for storing data transfer information was well known as evidenced by Yamagami et al., and since a data transfer register for storing data transfer information temporally store data of the storage units, an artisan would have been motivated to implement this feature in the system of Schiozaki et al.. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made by applicant, to modify the system of Schiozaki et al. to include a data transfer register for storing data transfer information since it was well known to temporally store data of the storage units (par.3, lines 5-6) as taught by Yamagami et al..

As per claims 2 and 10, Schiozaki et al. discloses a data transfer control unit comprising a plurality of data buffers and a plurality data transfer registers [*a storage control system using plural buffer arrays*; col.1, lines 7-8; *a first buffer array as a buffer storage directory for registering an address of data*; col.1, lines 9-11]; and when a second data transfer based on second data transfer information controlled while a first data transfer based on first data transfer information controlled, a data transfer control unit reads a second data transfer information from a second memory, writes a second data transfer information into a second data transfer register, and accordance with the second data transfer information, controls a second data transfer before a first data transfer information and data to be transmitted and received by a first data transfer are read from a first data transfer register storing a first data transfer information and a first data buffer storing the data be transmitted and received by a first data transfer and written in a second memory [*for a write (store) operation by another processor to the main storage, a request is issued to the second address array (control storage) and thereafter the first address array (control storage) is updated*; col.2, lines 12-16; *the data is read from the buffer memory; a transfer is executed from the main storage to the buffer storage*; col.2, lines 39-42; *a storage control system comprising a first buffer address array as a buffer storage directory for registering thereto an address of data copied from a shared storage into a buffer storage of each processor and a second buffer address array provided for a store address check requested from another processor;* col.1, lines 8-15; *access request in the second processor is accepted when a transfer from the shared storage to the buffer storage of the second processor is completed and the first buffer address array is updated in association with the transfer*; col.3, lines 31-36; *the processor accesses the buffer storage onto which data stored in the main storage*; col.1, lines 25-27;].

As per claims 3 and 11, Schiozaki et al. discloses the data transfer is controlled in unit of each data block obtained by dividing data to be transferred between a first storage control apparatus and a second control apparatus into least one or more data [*a first buffer address array (storage control) as a buffer storage directory for registering an address of data copied from a shared storage into a buffer storage of each processor and a second buffer address array (storage control) for a store address requested from another processor*; col.1, lines 9-15].

As per claims 4 and 12, Schiozaki et al. discloses first storage control apparatus connected to a second storage control apparatus communication enable state via at least one or more switches [*a first processor executes a store request on a main storage conducting communications with another system and a second processor fetches data stored*; col.2, lines 24-28; *Fig.2, control storage 4a, control storage 7a, Latches 51,58*].

As per claims 5 and 13, Schiozaki et al. discloses the data input/output request relative to a second storage volume is received from a information processing apparatus, a data transfer information is written in a second memory [*a transfer request received is compared with an MS request from another processor (including input/output units)*; col.4, lines 9-12]; and a data transfer control unit reads a data transfer information from a second memory, writes a data transfer information a data transfer register, and in accordance with a read data transfer information, controls data transfer when a data between a first memory and a second storage control apparatus [*the data is read from the buffer memory; a transfer is executed from the main storage to the buffer storage*; col.2, lines 39-42; *for a write (store) operation by another processor to the main storage, a request is issued to the second address array (control storage) and thereafter the first address array (control storage) is updated*; col.2, lines 12-16; *the first*

address array controller 4a issues a request via a line 13a to the SCU 2 to read data from the MS 3; col.4, lines 6-8].

As per claims 6 and 14, Schiozaki et al. discloses when a data write request relative to a first storage volume and write data are received from an information processing apparatus, an input/output control unit writes a data transfer information a second memory order to write copy volume [*for a write (store) operation by another processor to the main storage, an update request is issued first to the second address array when a fetch request is made to the main storage*; col.2, lines 12-16; *a transfer request received is compared with an MS request from another processor (including input/output units)*; col.4, lines 9-12]; and a write data into a second storage a data transfer control unit reads a data transfer information from a second memory, writes a data transfer information into a data transfer register, and in accordance with a read data transfer information, controls transmission of the write data from a first memory a second storage control apparatus [*the data is read from the buffer memory; a transfer is executed from the main storage to the buffer storage*; col.2, lines 39-42; *the first address array controller 4a issues a request via a line 13a to the SCU 2 to read data from the MS 3*; col.4, lines 6-8; *the second processor issues a request to read data stored at address X after the block transfer is completed, so the first address array is checked to determine whether or not the relevant data has been registered to the buffer storage*; col.3, lines 44-48].

4. Claims 7-8, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiozaki et al. (4,683,533) in view of Yamagami et al. (2002/0194435), and further in view of Yanai et al. (5,742,792).

As per claims 7 and 15, Schiozaki et al. discloses the first memory stores data to be received at least between the first apparatus and the information processing apparatus or the second storage control apparatus [*a first control storage (address array) and second control storage (address array)*; col.2, lines 1-3; *for a write (store) operation by another processor to the main storage, a request is issued to the second address array (control storage) and thereafter the first address array (control storage) is updated*; col.2, lines 12-16; *a first processor executes a store request on a main storage conducting communications with another system and a second processor fetches data stored*; col.2, lines 24-28]; an input/output control unit writes data transfer information in a second memory, a data transfer information containing the storage location of data a first memory and a storage location of data in the information processing apparatus or the second storage apparatus [*a block transfer request received via the line 13a is compared with an MS request from another processor (including input/output units) for accessing the MS 3 in the SCU 2*; col.4, lines 9-13; *the SCU 2 has a line 16a connected to the first address array controller 4awhich is used to indicate a transfer from the MS 3 to the BS 6a; the SCU is connected to a second address array controller 7a associated with the processor 1a and to a second address array controller 7b*; col.4, lines 19-26]; and data transfer control unit controls data transfer between the first memory and the information processing apparatus or the second storage control apparatus via the data buffer in accordance with the data transfer information read from the second memory and written in the data transfer register [*controllers 7a and 7b being provided with buffer address arrays*; col.4, lines 27-29; *a storage control system comprising a first buffer address array as a buffer storage directory for registering thereto an address of data copied from a shared storage into a buffer storage of each processor and a second buffer address array provided for a store address check requested from another processor;* col.1, lines 8-15].

However Schiozaki et al. does not specifically teach a cache memory unit having a circuit board formed with a first memory, and a disk control unit for reading/writing data relative to a first storage volume as recited in the claim.

Yamagami et al. discloses and a cache memory unit having a circuit board formed with the first memory [*and a cache memory that temporally stores data of the storage units;* par.3, lines 5-6; *the two or more storage directors are connected to the cache memory and each of the storage directors has an access path to the cache memory*; par.3, lines 6-8]; a disk control unit for reading/writing data relative to a first storage volume [*disc control unit has storage directors each of which controls data transfers (read/write) between a CPU and a storage unit*; par.3, lines 2-5] to temporally store data of the storage units (par.3, lines 5-6).

Since the technology for implementing a storage control apparatus with a cache memory and a disc control unit was well known as evidenced by Yamagami et al., and since a cache memory and a disc control unit temporally store data of the storage units, an artisan would have been motivated to implement this feature in the system of Schiozaki et al.. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made by applicant, to modify the system of Schiozaki et al. to include a cache memory and disc control unit since it was well known to temporally store data of the storage units (par.3, lines 5-6) as taught by Yamagami et al..

However Schiozaki et al. and Yamagami et al. do not specifically teach a channel control unit having a circuit board formed with a second memory, an input/output control unit and a data transfer control unit.

Yanai et al. discloses a channel control unit having a circuit board formed with a second memory, an input/output control unit and a data transfer control unit [*Fig.1, channel control unit 26, controller 16, second memory 22b, input/output control unit (communicative link 40), data transfer control unit (internal bus 38, communication bus 70)*] to control the operation of a data storage system controller (col.8, lines 6-7).

Since the technology for implementing a storage control apparatus with a channel control unit having a circuit board formed with a second memory, an input/output control unit and a data transfer control unit was well known as evidenced by Yanai et al., and since a channel control unit having a circuit board formed with a second memory, an input/output control unit and a data transfer control unit control the operation of a data storage system controller, an artisan would have been motivated to implement this feature in the system of Schiozaki et al. and Yamagami et al.. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made by applicant, to modify the system of Schiozaki et al. and Yamagami et al. to include a channel control unit having a circuit board formed with a second memory, an input/output control unit and a data transfer control unit since it was well known to control the operation of a data storage system controller (col.8, lines 6-7) as taught by Yanai et al..

As per claim 8, Schiozaki et al. discloses a storage control apparatus for a storage system comprising a first storage control apparatus for receiving a data input/output request from an information processing apparatus and performing a data input/output process relative first storage volume for storing data and a second storage control apparatus connected to a first storage control apparatus communication enable state via at least one or more switches for performing a data input/output process relative to a second storage volume storing data, a first storage control apparatus comprises: a cache memory unit having a circuit board formed with first memory for storing data transferred at least between a first storage apparatus and an information processing apparatus or a second storage control apparatus [*a storage control system*; col.1, lines 6-8; *a transfer request received is compared with an MS request from another processor (including input/output units)*; col.4, lines 9-12; *a first control storage (address array) and second control storage (address array)*; col.2, lines 1-3; *for a write (store) operation by another processor to the main storage, a request is issued to the second address array (control storage) and thereafter the first address array (control storage) is updated*; col.2, lines 12-16; *a first processor executes a store request on a main storage conducting communications with another system and a second processor fetches data stored*; col.2, lines 24-28; *a first processor executes a store request on a main storage conducting communications with another system and a second processor fetches data stored*; col.2, lines 24-28; *Fig.2, control storage 4a, control storage 7a, Latches 51,58;*]; second memory [*a second address array for storing data*; col.1, lines 51-52]; an input/output control unit for writing data transfer information in a second memory, a data transfer information containing a storage location of data in a first memory and a storage location of data in the information processing apparatus or the second storage control apparatus [*a block transfer request received via the line 13a is compared with an MS request from another processor (including input/output units) for accessing the MS 3 in the SCU 2*; col.4, lines 9-13; *the SCU 2 has a line 16a connected to the first address array*

controller 4awhich is used to indicate a transfer from the MS 3 to the BS 6a; the SCU is connected to a second address array controller 7a associated with the processor 1a and to a second address array controller 7b; col.4, lines 19-26]; a data transfer control unit having a plurality data buffers for storing data and a plurality of data transfer registers for storing a data transfer information, and controlling data transfer between a first memory and an information processing apparatus or a second storage control apparatus via a data buffer in accordance with a data transfer information read from a second memory and written a data transfer register [*a storage control system using plural buffer arrays*; col.1, lines 7-8; *a first buffer array as a buffer storage directory for registering an address of data*; col.1, lines 9-11; *a storage control system comprising a first buffer address array as a buffer storage directory for registering thereto an address of data copied from a shared storage into a buffer storage of each processor and a second buffer address array provided for a store address check requested from another processor;* col.1, lines 8-15; *data is read from the buffer memory; a transfer is executed from the main storage to the buffer storage*; col.2, lines 39-42]; when second data transfer based on second data transfer information is controlled while first data transfer based on first data transfer information is controlled, a data transfer unit reads a second data transfer a second control information from memory, writes a second data transfer information into a second data transfer register, and in accordance with the second data transfer information, controls a second data transfer before a first data transfer information and data to be transmitted and received by a first data transfer are read from a first data transfer register storing a first data transfer information and a first data buffer storing data to be transmitted and received by a first data transfer and written a second memory [*access request in the second processor is accepted when a transfer from the shared storage to the buffer storage of the second processor is completed and the first buffer address array is updated in association with the transfer*; col.3, lines 31-36; *the processor accesses the*

buffer storage onto which data stored in the main storage; col.1, lines 25-27; *data is read from the buffer memory; a transfer is executed from the main storage to the buffer storage*; col.2, lines 39-42].

However Schiozaki et al. does not specifically teach a disk control unit for reading/writing data relative a first storage volume as recited in the claim.

Yamagami et al. discloses a disk control unit for reading/writing data relative a first storage volume [*disc control unit has storage directors each of which controls data transfers (read/write) between a CPU and a storage unit*; par.3, lines 2-6]; a plurality of data transfer registers for storing the data transfer information [*registers 340a and 340b are provided in correspondence to the respective SM access paths 125 and communication with the SM unit 160 can be ensured by reading/writing the registers 340a and 340b*; Fig.3, REG#0-REG#7; par.105, lines 1-6] to temporally store data of the storage units (par.3, lines 5-6).

Since the technology for implementing a storage control apparatus with a disc control unit was well known as evidenced by Yamagami et al., and since a disc control unit temporally store data of the storage units, an artisan would have been motivated to implement this feature in the system of Schiozaki et al.. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made by applicant, to modify the system of Schiozaki et al. to include a disc control unit since it was well known to temporally store data of the storage units (par.3, lines 5-6) as taught by Yamagami et al..

However Schiozaki et al. and Yamagami et al. do not specifically teach a channel control unit having a circuit board formed with a data transfer control unit.

Yanai et al. discloses a channel control unit having a circuit board formed with a data transfer control unit [*Fig.1, channel control unit 26, controller 16, second memory 22b, input/output control unit (communicative link 40), data transfer control unit (internal bus 38, communication bus 70)*] to control the operation of a data storage system controller (col.8, lines 6-7).

Since the technology for implementing a storage control apparatus with a channel control unit having a circuit board formed with a data transfer control unit was well known as evidenced by Yanai et al., and since a channel control unit having a circuit board formed with a data transfer control unit control the operation of a data storage system controller, an artisan would have been motivated to implement this feature in the system of Schiozaki et al. and Yamagami et al.. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made by applicant, to modify the system of Schiozaki et al. and Yamagami et al. to include a channel control unit having a circuit board formed with a data transfer control unit since it was well known to control the operation of a data storage system controller (col.8, lines 6-7) as taught by Yanai et al..

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Schiozaki et al.	4,683,533
Yamagami et al.	2002/0194435
Yanai et al.	5,742,792

6. When responding to the office action, Applicant is advised to clearly point out the patentable novelty that he or she thinks the claims present in view of the state of the art disclosed by references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111(c).

7. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mardochee Chery whose telephone number is (571) 272-4246. The examiner can normally be reached on 8:30A-5:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Manonama Padmanabhan can be reached on (571) 272-4210. The fax

phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

April 1, 2005

MC

Mardochee Chery
Examiner
AU: 2188

Pierre M. Vital

Pierre M. Vital
Primary Examiner
AU 2188